Optimize Power of CMOS Multiplexer based Combinational Circuit using Sleepy Keeper Technique

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Abstract

Power optimization in CMOS-based combinational circuits is a critical area of research in low-power VLSI design, especially with the increasing demand for energy-efficient digital systems. This study focuses on optimizing the power consumption of CMOS multiplexer-based combinational circuits using the Sleepy Keeper Technique, an advanced leakage power reduction approach. The Sleepy Keeper Technique employs a combination of sleep transistors and keeper logic to effectively minimize leakage power while maintaining the circuit's logic state during standby mode. By integrating this technique into CMOS multiplexers, the proposed design achieves a significant reduction in static power dissipation, making it suitable for low-power applications in processors, communication systems, and embedded devices. To evaluate the effectiveness of this approach, the proposed design is implemented and analyzed in terms of power consumption, propagation delay, and area overhead. Simulation results demonstrate that the Sleepy Keeper-based CMOS multiplexer outperforms conventional designs by achieving a substantial reduction in leakage power with minimal impact on performance metrics.

This research highlights the potential of the Sleepy Keeper Technique in enhancing the energy efficiency of multiplexer-based combinational circuits, paving the way for power-aware digital architectures in next-generation VLSI systems. Future work can explore further scalability, adaptive power gating, and hybrid leakage reduction strategies to improve power efficiency in deep submicron and nanoscale CMOS technologies.

Keywords: Sleep Keeper (SK), AND_OR, NAND_NOR, CMOS

I. INTRODUCTION

In modern VLSI design, reducing power consumption is a critical challenge, especially with the increasing demand for energy-efficient and high-performance digital circuits. CMOS-based combinational circuits, particularly multiplexer-based designs, are widely used in processors, data processing units, and communication systems due to their efficient logic operations. However, as transistor dimensions shrink in deep submicron technologies**,** leakage power dissipation has become a major concern, significantly affecting circuit performance and reliability.

To address this issue, various power reduction techniques have been developed, with the Sleepy Keeper Technique emerging as a promising solution for leakage power minimization**.** This method integrates sleep transistors and a keeper circuit to reduce static power dissipation while maintaining the circuit's logic state during idle periods. The Sleepy Keeper approach enhances power efficiency without introducing excessive delay, area overhead, or performance degradation, making it highly suitable for low-power VLSI applications.

This research focuses on implementing CMOS multiplexer-based combinational circuits using the Sleepy Keeper Technique and evaluating its impact on power consumption, delay, and circuit efficiency. The primary objectives of this study are:

To design and implement CMOS multiplexers integrated with the Sleepy Keeper Technique.

To analyze and compare power consumption, leakage current, and performance metrics with conventional CMOS circuits.

To explore trade-offs between power optimization, area utilization, and timing constraints.

II. PULL-UP AND PULL DOWN

Pull-up network (PUN) and pull-down network (PDN) are two networks that form a static CMOS gate. Figure 1 shows a normal N-input logic input where all information is passed to

both the draw-up and pull-down organisations. PUN is always used to connect the output to ground. The output of the logic gate should be 1 (based on the input). If the output of a logic gate is to be zero, the PDN connects the logic gate to a voltage source. In mutually exclusive networks, pull-up and pull-down networks are constructed to be in a stable state. Thus, when the drifter is stable, there is usually a path between ground and the result F, which means a high result ("1"), and conversely between the voltage source and F, which means a low result ("zero"). In steady state.

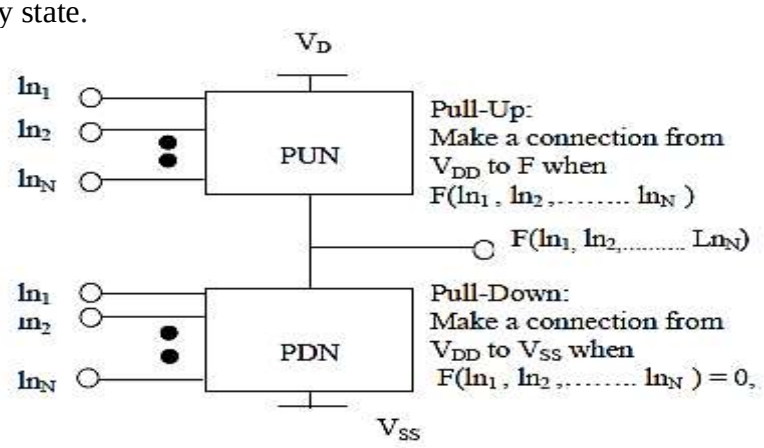
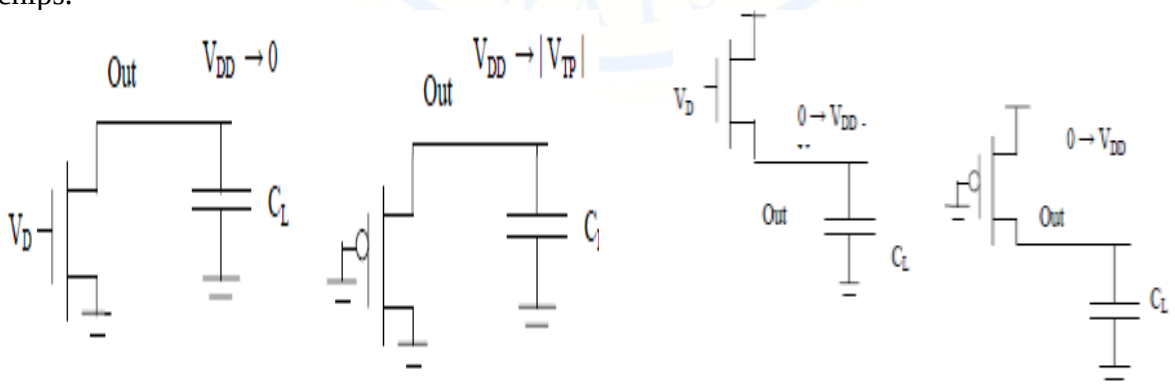


Fig. 1: PUN and PDN

The gate signal of the transistor can be used to control the switch. When the control signal is high, the NMOS switches on, and when the control characteristic is low, the NMOS switches off, the inverting switch is provided by a PMOS transistor. The PMOS switch is on when the control signal is low and off when the control signal is high. NMOS devices are used in drawdown configurations and PMOS semiconductors are used in drawdown configurations. The main reason is that PMOS devices generate a "strong 1" whereas NMOS transistors generate a "strong 0". To see how this works, look at the example in Figure 2.

The resulting capacitance is initially charged to VDD in Figure 2a. There are two examples of unload scenarios: NMOS semiconductors are generally preferred as PDN. Essentially, Figure 2b shows two alternative ways of powering a capacitor, with the capacitor voltage initially at GND. A PMOS switch charges the capacitor up to VDD in this way, but an NMOS device cannot boost the capacitor beyond VDD-VTn. Hence, PMOS semiconductors are also used in chips.



(a) (b)

Fig. 2: NMOS and PMOS Switches

III. PROPOSED METHODOLOGY

For this encryption, AND_OR & NAND_NOR with key has developed. The AND_OR gate with key is present in fig. 3, the key is '0' than circuit like a AND gate & '1' than circuit like a OR gate. The NAND_NOR gate with key is present in fig. 4, the key is '0' than circuit like a NAND gate & '1' than circuit like a NOR gate.

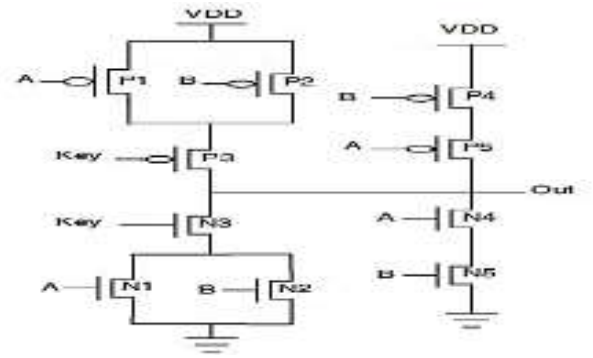


Fig. 3: AND_OR

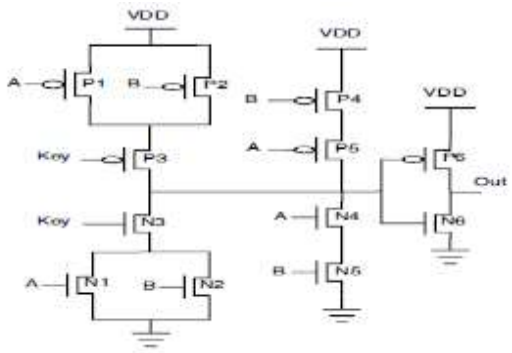


Fig. 4: NAND_NOR

3.1 Sleepy Keeper

We present a new method for reducing overflows, called the "sleepy keeper" approach. This section details the structure and functionality of the Sleepy Keeper approach. We also discuss layout issues for the Sleepy Keeper strategy. The main problem with traditional CMOS is the efficient use of transistors. PMOS semiconductors are used for the VDD power supply and NMOS semiconductors are grounded. However, PMOS semiconductors are less efficient when they pass GND at the same time. Therefore, NMOS semiconductors are less efficient when they pass VDD. The sleep keeper method uses an initial value of 1 to maintain the level "1" during sleep. The NMOS semiconductor is connected to VDD, and the output value is maintained at "1" during sleep mode. The amplifying single NMOS semiconductor connected to both ends of the pull-up static semiconductor passes VDD to the pull-up organization. During sleep, the sleep transistor is disabled so this NMOS transistor serves as the only VDD power source.

An additional single NMOS semiconductor, installed in-line with the pull-down residual semiconductor, connects VDD to the pull-down network as shown in Figure 5. During sleep mode, the remaining semiconductor is disabled so this NMOS semiconductor serves as the main VDD power source for the pull-down network. One additional PMOS transistor is placed above the pull-down network as shown in Figure 3.8. During sleep, the sleep transistor is disabled so this NMOS transistor serves as the only VDD power source. This is a duplicate instance of case "1" above. For this method to work, it is only necessary that the NMOS connected to VDD and the PMOS connected to GND are able to maintain the corresponding logic state. This seems possible because other researchers have described ways to maintain the logic state at significantly lower VDD values. For example, we propose a significantly lowered VDD value that is sufficient to maintain the state. The slow guard semiconductors (NMOS connected to VDD and PMOS connected to GND) are never used to significantly change the output voltage. They are only used to maintain a well-determined output voltage. In particular, the slowly acting guard transistors act as the only connections that maintain the same output voltage for a few clock cycles after going to sleep and before waking up.

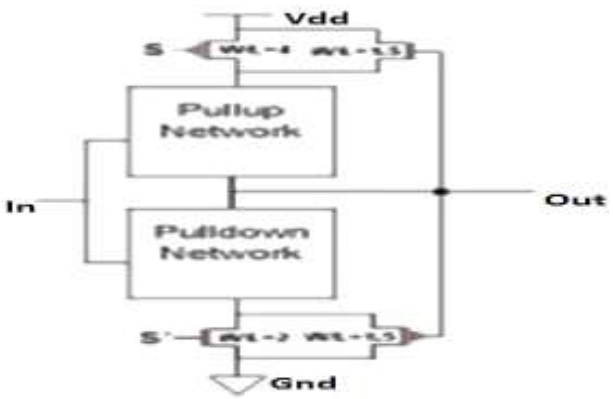


Fig. 5: SK approach

IV. RESULTS

Speed and power consumption are in conflict with each other. When speed is given top priority, the limiting voltage is usually reduced and the storage voltage is increased. When power dissipation is given priority, the limiting voltage is increased and the storage voltage is reduced. We have designed all design on 45n and 65n technology.

Create NAND_NOR design using SK technique on DSCH in present in fig. 6 and draw TD in figure 7. Layout of NAND_NOR is design using SK technique in present in fig. 8. The NAND_NOR CMOS provide a 0.363 mw µw for 90n is present in figure 9.

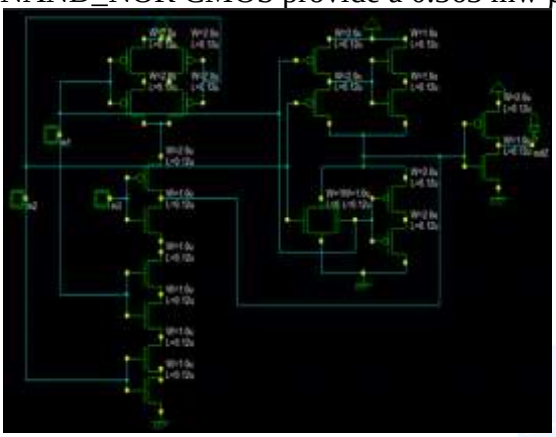


Fig. 6: NAND_NOR Gate using SK

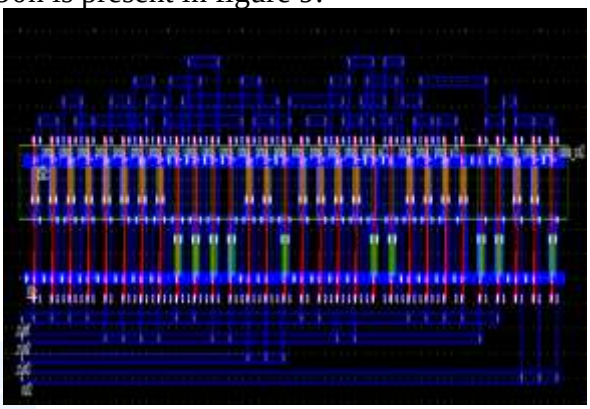


Fig. 8: Layout of NAND_NOR Gate using SK

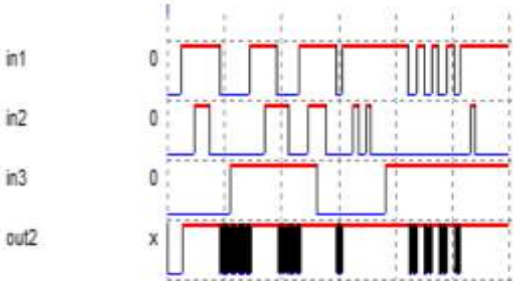


Fig. 7: TD of NAND_NOR Gate using SK

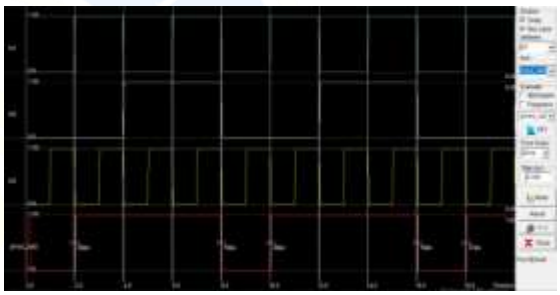


Fig. 9: PD of NAND_NOR Gate for 90n using SK

Create AND_OR design on DSCH in present in fig. 10 and draw TD in figure 11. Layout of AND_OR design in present in fig. 12. The AND_OR CMOS provide a 0.403 mw for 90n is present in figure 13.

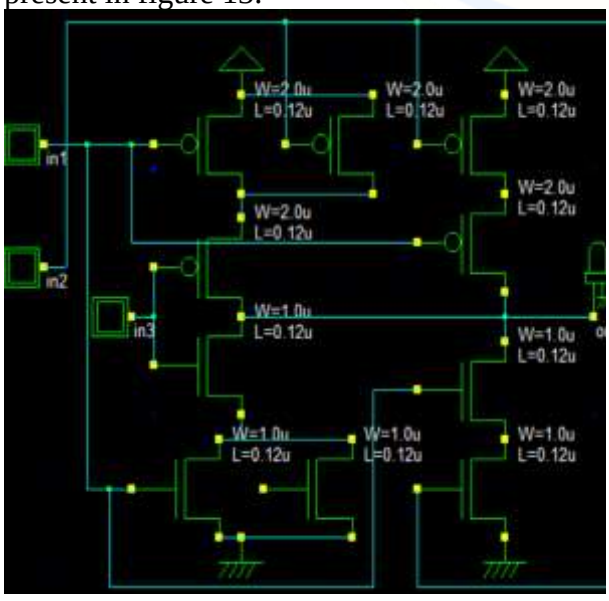


Fig. 10: AND_OR Gate

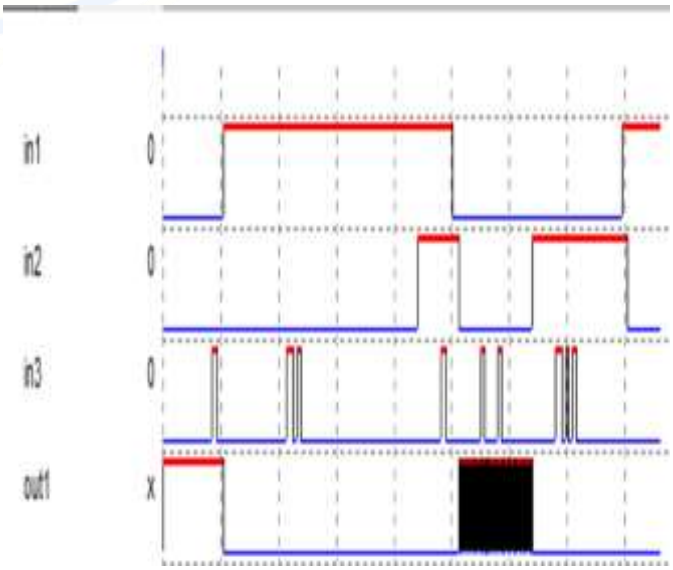


Fig. 11: TD of AND_OR Gate

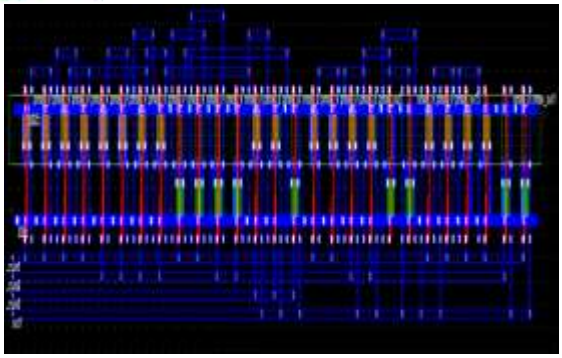


Fig. 12: Layout of AND_OR Gate

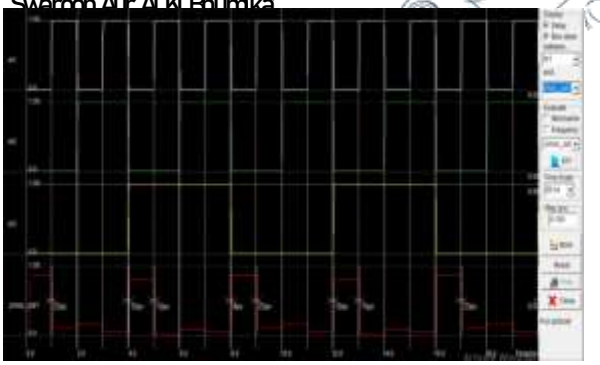


Fig. 13: PD of AND_OR Gate for 90n

V. CONCLUSION

The implementation of the Sleepy Keeper Technique in CMOS multiplexer-based combinational circuits demonstrates a significant reduction in leakage power dissipation while maintaining circuit stability and functionality. By integrating sleep transistors and keeper logic, this approach effectively reduces static power consumption without severely impacting performance metrics such as propagation delay and area overhead.

Simulation results confirm that the proposed design outperforms conventional CMOS multiplexer architectures in terms of power efficiency, making it highly suitable for low-power VLSI applications **in** processors, embedded systems, and communication devices**.** The study also highlights the trade-offs between power saving and circuit performance, emphasizing the need for further optimization in deep submicron and nanoscale CMOS technologies.

Future work can explore adaptive power gating strategies**,** hybrid leakage reduction techniques**, and** scalability to advanced technology nodes to further enhance energy efficiency. The findings of this research contribute to the development of next-generation power-aware CMOS designs**,** enabling more efficient and sustainable digital systems in modern computing and electronics.

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