Design and Implementation of Efficient Hybrid Form FIR Filters with Variable Approach

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Abstract:

Finite Impulse Response (FIR) filters are popular due to their attractive properties such as linear phase characteristic and stability, but traditional implementation methods can result in high computational complexity. To address this, hybrid form FIR filters have been proposed that combine the advantages of different forms. We propose an efficient implementation of hybrid form FIR filters that utilizes variable size partitioning to divide the filter into sub-filters of different lengths, each implemented using a suitable structure. The effectiveness of the proposed approach is demonstrated through experimental results, showing significant performance improvement while maintaining low computational cost. The simulation result shows that the normal power consumption is reduced by 30.44% in comparison to traditional structure. Thus the proposed approach is well-suited for practical applications where real-time implementation and low power consumption are critical factors.

Keywords: ***Finite Impulse Response (FIR), Linear Phase Architecture (LPA), Real time digital processing, Pipelining and parallel Architecture, Data Flow Graph (DFG).***

1. Introduction

Finite Impulse Response (FIR) filters have gained significant attention due to their attractive properties such as linear phase response, stability, and easy implementation. However, traditional FIR filter implementation methods often lead to high computational complexity, particularly for long filter lengths. To address this issue, several techniques have been proposed, including hybrid form FIR filters that combine different implementation structures to achieve optimal performance. Hybrid Form FIR Filters with Variable Partitioning Approach is an advanced signal processing technique that is widely used in various applications, such as image processing, audio processing, and communication systems. The hybrid form filter combines the advantages of two different forms of FIR filters, namely direct form and cascade form, to achieve better performance in terms of speed, accuracy, and resource utilization. Efficient Implementation of Hybrid Form FIR Filters with Variable Partitioning Approach is a method of implementing the hybrid form filter that optimizes the partitioning scheme of the filter coefficients to minimize the computation time and memory usage while maintaining a desired level of

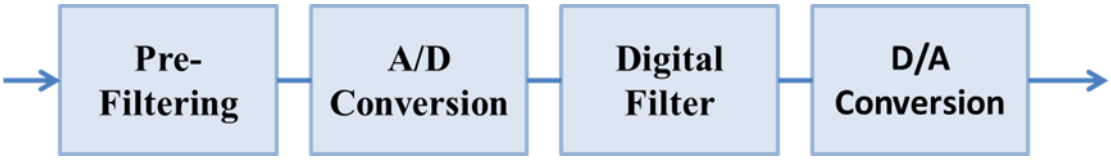

Figure 1 Block diagram of signal filtering

performance. This approach allows for adaptive partitioning of the filter coefficients, which means that the filter can dynamically adjust the partitioning scheme based on the input signal characteristics, resulting in improved filter efficiency.

In this paper, we propose an efficient implementation of hybrid form FIR filters that utilize a variable size partitioning approach. The proposed approach is based on dividing the filter into sub-filters of different lengths, each implemented using a suitable structure. The choice of the structure is made based on the length of the sub-filter, resulting in a more efficient implementation with reduced computational complexity.

The effectiveness of the proposed approach is demonstrated through experimental results, which show that the proposed method achieves significant performance improvement over traditional methods while maintaining a low computational cost. This makes the proposed approach well-suited for practical applications where real-time implementation and low power consumption are critical factors.

The remaining contains are organized as follows. In section 2, the related work is presented. Section 3, outlined the methodology to design the traditional FIR structure. The hybrid form of low pass FIR filter design is discussed in section 4. Then, in Section 5, results are presented where the proposed structure is compared with the traditional hybrid form FIR filter. Finally, the conclusions are given in section 6.

2. Related work

Efficient implementation of hybrid form FIR filters with variable size partitioning approach has been a topic of interest in the field of digital signal processing. Several research works have been done in this area to improve the efficiency and speed of FIR filters. Another approach is to use hybrid forms of FIR filters, which combine the advantages of both symmetric and asymmetric filters. These filters have a better frequency response than symmetric filters and require fewer coefficients than asymmetric filters [1]. They also have a linear phase response, which is an important requirement in many applications. Sumbal Zahoor at el, [2] has presented a new methodology for designing optimized FIR digital filters from software to hardware level, with the goal of reducing arithmetic complexity and hardware resources. The Kaiser window and direct-form structure are recommended for their performance and simplicity, and the optimized filter implementation requires 42% less hardware resources than a normal implementation. Power efficient structure of FIR filter has given overview [3-5].

A Chandra at el, [6] provides an overview of the state-of-the-art research in the field of hardware-efficient multiplier-less FIR digital filter design. It covers various conventional techniques, improved variants, and intelligent optimization techniques for designing such filters, and suggests that a trade-off between design objectives is essential. The article also proposes future research directions, including multi-objective optimization algorithms and the application of fuzzy logic to designing powers-of-two filters. The paper concludes by highlighting the importance of hardware-efficient digital filter design and its potential applications in communication and signal processing fields. Wen B. Y. at el,[7] proposed a novel evolutionary algorithm (GA) for creating linear phase FIR filters without coefficient multipliers. These filters have a cheap hardware cost since adders and shifts are used in place of the coefficient multipliers. To maximise the probability of finding viable options and shorten computing time, the suggested GA divides the discrete search space into smaller ones. A new fitness function is proposed that places more emphasis on minimising hardware cost and is suited for the partitioned search spaces. The article also introduces unique integer polynomial factorization techniques for building cascade form FIR filters, as well as adaptive crossover and mutation rates. The suggested algorithm is contrasted with competing methods, and many design examples are used to illustrate its superiority. C. H. Chang at el, [8] presented an analysis of the Canonical Signed Digit based method to add two numbers with minimal logical depth (LD). The study shows that because the nonzero digits in the addends have been submerged, changed to distinct signed digit (SD), and shifted in position, the CSE algorithm cannot uncover all advantageous common patterns from any SD representation of the coefficient set. This understanding serves as the foundation for the article's new algorithm proposal, the minimum LD Grey to Decimal algorithm, which is favourably compared to the most recent GD algorithm. The anticipated power is reduced by up to 3.4 times due to the limited Logic Overhead in the suggested approach. D. Shi at el, [9] proposed a new algorithm for designing linear phase FIR filters in cascade form with discrete coefficients. The algorithm decomposes the overall filter into subfilters during the search process and achieves significant cost and adder depth reductions compared to single-stage designs. The authors also note that symmetric subfilters outperform non-symmetric ones, and increasing the filter length and coefficient word length can result in fewer adders and lower adder depth. The efficient constant multiplication methods have suggested [10-12].

3. **Methodology:** There are several methods that can be used for the efficient implementation of Hybrid Form FIR Filters with Variable Partitioning Approach. Here are some of the commonly used methods:

1. Fixed-point arithmetic: This method uses fixed-point arithmetic instead of floating-point arithmetic to reduce the computational complexity and memory usage of the filter. Fixed-point arithmetic is less resource-intensive than floating-point arithmetic, making it ideal for implementing filters on resource-constrained platforms [13].
2. Bit-level optimization: This method involves optimizing the filter implementation at the bit-level to reduce the number of arithmetic operations required for filter processing. This can be achieved by minimizing the number of adders and multipliers required for the filter implementation.
3. Pipeline processing: This method involves dividing the filter implementation into smaller processing blocks that can be processed in parallel. This can significantly reduce the processing time required for the filter implementation, making it more efficient.
4. Fast algorithms: There are several fast algorithms that can be used for the efficient implementation of Hybrid Form FIR Filters with Variable Partitioning Approach, such as the FFT-based algorithm and the polyphase decomposition algorithm. These algorithms can reduce the computational complexity of the filter implementation, making it faster and more efficient.
5. Hardware implementation: This method involves implementing the filter using hardware-based solutions, such as FPGAs and ASICs. Hardware implementations can provide faster processing times and lower power consumption compared to software-based implementations [14].

By using these methods, it is possible to implement Hybrid Form FIR Filters with Variable Partitioning Approach in an efficient and resource-friendly manner, making it ideal for real-time signal processing applications.

4. Proposed a Computationally Efficient Hybrid Form of FIR Filter Structure

In many DSP systems, FIR filters are frequently used. The transfer function of an Nth-order FIR filter can be expressed as

The transfer function for a FIR filter given in (1) can be divided into subsections of M taps

$$H(z) = \sum_{i=0}^{N} h_i z^{-i} \quad \textbf{(1)}$$

and recast, assuming that N + 1 is an integer multiple 2 of M, as shown in

$$H(z) = \sum_{k=0}^{\frac{(N+1)}{M}-1} \left[\sum_{i=0}^{M-1} h_{Mk+i}\, z^{-i} \right] z^{-Mk} \quad \textbf{(2)}$$

Rearranging the values in (2) results in

$$H(z) = \sum_{i=0}^{M-1} \left[\sum_{k=0}^{\frac{(N+1)}{M}-1} h_{Mk+i}\, z^{-i} \right] z^{-i} \quad \textbf{(3)}$$

which is equivalent to the polyphase decomposition of the transfer function. The structure of the polyphase decomposed FIR filter is as

$$H(z) = \sum_{k=0}^{\frac{(N+1)}{M}-1} h_{Mk+i}\, z^{-Mk} \quad \textbf{(4)}$$

This is the same as the shown in (1). It should be noted that the filter structure is the same for M = 1 as it is for M = N + 1, which corresponds to the direct form FIR filter. The transposed direct form filter in Fig. 1 (b) has M - 1 equally spaced delay elements that have been retimed

from the lower (output) branch to the upper (input) branch. The final structure must then incorporate a matrix multiplication as a result of extra retiming [15].
The filter structure depicted in Figure 2 has equivalent numbers of multipliers, adders, and delay elements to any of the structures as long as N+1 is a multiple of M. However, similar to the traditional hybrid form FIR filters, the critical path is reduced compared to the direct form filter, and the number of wide delay elements is lower than that of the transposed form FIR filter. Additionally, instead of having multiple smaller MCM blocks as in the traditional hybrid form FIR filter, there is now one matrix MCM block. This not only enables the use of redundancies within a row or column of coefficients, but also between entire rows or columns [16].

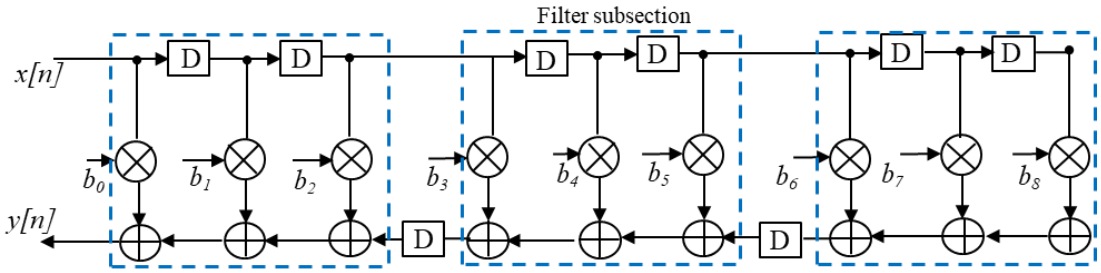

Figure 2 Eight-order FIR filter structure in hybrid form

5. Results and Discussion

A FPGA in the Virtex 4 family is used to synthesise the updated structure that has thus been built, as shown in Table 1, by combining the suggested methods based filter operations.
The results of comparing a proposed hybrid form FIR filter with a traditional transpose form FIR filter, using different order that varies from 8 to 128 FIR filter are presented as shown in Table 1.
The introduced hybrid form filter, the number of delay elements may be significantly larger for certain values of M, which is typically a large value. Despite this, the proposed filter structure reduces the number of adders compared with the traditional transpose form filter. The traditional form requires fewer adders for M = 1 and 64 because the algorithm produces better results for those values of M than the algorithm in [6].

Table 1 Comparative chart of power consumption

S.No	Filter order	Filter structure in Direct form(mW)	Filter structure in Transpose(mW)	Filter structure in **Hybrid form**(mW)	Ratio of Structure-Proposed/Transpose
1.	8	234	283	160	43.46%
2.	16	297	324	208	35.80%
3.	32	338	375	269	28.26%
4.	64	385	413	321	22.27%
5.	128	419	481	373	22.45%
Reduction in average power consumption					**30.44%**

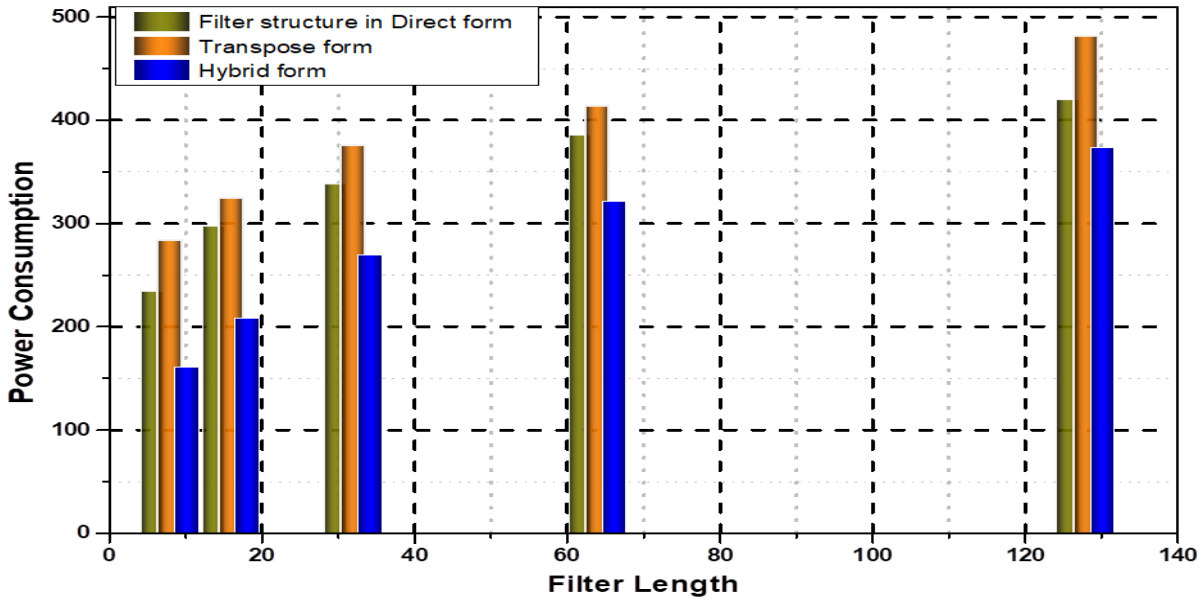

Fig.3.Average power consumption

The suggested filter structure with flexible architecture is compared to an existing filter structure in terms of power consumption, as shown in Fig. 3. When compared to existing filter topologies, the average power of the proposed FIR filter for various filter lengths Table 2 shows the outcomes. When compared to the traditional form, it is found that the power consumption for the proposed design has been lowered by 30.44%.

6. Conclusion

A hybrid form FIR filter construction that enables the usage of matrix multiple constant multiplication (MCM) blocks was taken into consideration in this work. A special case of a polyphase decomposed filter with shared delay components for the sub filters is used to design hybrid form FIR filter. The proposed approach uses less adders than the conventional transpose form filter, as demonstrated. The critical path, the maximum fan-out for a node, and the quantity of broader delay elements can all be traded for one another in hybrid form FIR filters, which has advantages over direct and transposed direct form filters in terms of power usage. The proposed structure appears to have potential as an attractive alternative because it simultaneously obtains the complexity reduction of MCM and the trade-off possibilities of hybrid form filters. However, further examination on the circuit level must be done. This is a combination of things that was previously impossible. Further, the use of MCM blocks in hybrid form FIR filter design can result in more efficient implementations with fewer multipliers and adders required for implementation. However, the choice of algorithm used for the design and the distribution of extra zeros can affect the quality of the results obtained.

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